REMARKS

Entry of this Amendment is proper because it merely narrows the issues on appeal and does not require further search by the Examiner.

Claims 29-39 and 41-49 are all the claims presently pending in the application. Claims 29, 41, and 45-46 have been amended to more particularly define the invention. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claims 29, 34, 41, 42 and 45-46 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tanigawa (U.S. Patent No. 5,740,099). Claims 29, 34, 35, 41, 42 and 45-46 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Okonogi (U.S. Patent No. 5,529,947). Claims 30-33, 36-39, 43-44, and 47-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanigawa in view of Okonogi (U.S. Patent No. 5,529,947). Claims 30-33, 36-39, 43-44 and 47-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Okonogi.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device which includes a bulk silicon region comprising single crystal silicon and a silicon-on-insulator (SOI) region. Further, the SOI region includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer. Moreover, a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

Conventional substrates having an SOI region are formed either by separation by

implantation of oxygen (SIMOX) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, neither of these processes can form an insulator layer having a sidewall which is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

The claimed device, on the other hand, has an insulator layer having a sidewall which is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer. Therefore, unlike conventional devices, the claimed device has an insulator layer with a sidewall angle which may be easily controlled to reduce a sharp corner stress.

III. THE PRIOR ART REFERENCES

A. The Tanigawa Reference

The Examiner alleges that Tanigawa discloses the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Tanigawa.

Tanigawa discloses a semiconductor dynamic random access memory device has a memory cell array fabricated on a silicon-on-insulator (SOI) region and peripheral and interface circuits fabricated on a bulk region. The SOI region is formed by a separation by implantation of oxygen (SIMOX) process (Tanigawa at Abstract).

However, Applicant submits that Tanigawa does not teach or suggest "wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer" as recited in claims 29, 41 and 45-46. As noted above, conventional substrates having an SOI region are formed either by separation by implantation of oxygen (SIMOX) (Application at page 5, lines 2-10) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, with these processes it is difficult to form an insulator layer having a sidewall which is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

The claimed device, on the other hand, has an insulator layer having a sidewall which is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer (Application at Figures 1D and 2A). Therefore, unlike conventional devices, the claimed device has an insulator layer with a sidewall angle which may be easily controlled to reduce a sharp corner stress (Application at page 8, lines 17-21).

More specifically, referring to Figure 2A, the Application explains that the insulator layer in the claimed device may be formed by etching a groove having an angled sidewall and a depth of about 1000Å to 5000Å in a bulk silicon substrate 11 (Application at page 8, lines 17-20). For example, the sidewall angle may be easily controlled to about 103° to reduce sharp corner stress. The groove may then be filled with an insulating material to form the insulator layer with an angled sidewall (Application at Figure 2B).

Clearly, Tanigawa does not teach or suggest these novel features. Indeed, Tanigawa merely teaches a well-known SIMOX process which is discussed in the Background section of the Application (Tanigawa at col. 8, lines 13-36). However, as noted above, in a SIMOX process a sidewall angle of an insulator layer would be difficult to control. Note for example, that Tanigawa does not disclose an angled sidewall on the insulator layer 30c (Tanigawa at Figure 6). Instead, Tanigawa merely shows the insulator layer 30c having no angled sidewall. Therefore, the Tanigawa device is likely to experience a sharp corner stress affecting the performance of the device.

Therefore, Applicant submits that Tanigawa does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Okonogi Reference

The Examiner alleges that Okonogi discloses the claimed invention, and that Okonogi would have been combined with Tanigawa to form the claimed invention. Applicant submits, however, that there are elements of the claimed invention that are not taught or suggested by Okonogi. Further, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Okonogi discloses a semiconductor device having an SOI region which is formed by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. The SOI region includes a silicon dioxide layer having gradually tapered peripheral edge (tapered wall) to reduce a local concentration of a stress (Okonogi at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters, different problems, and after completely different solutions from each other, let alone those of the claimed invention. Specifically, Tanigawa is directed to a well-known SIMOX process in which an insulator layer sidewall angle cannot be controlled, whereas Okonogi is directed to a process which seeks to control an insulator layer sidewall angle (Okonogi at Abstract). Clearly, these reference teach away from each other and would not have been combined by one of ordinary skill in the art.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious ... to use planarized isolation oxides and single crystal silicon in Tanigawa's device in order to simplify the processing steps of making the device, and providing better island isolation via trench isolation". Thus conclusory statement is believed insufficient to support the combination of the disparate references of Okonogi and Tanigawa.

Moreover, like Tanigawa, Okonogi does not teach or suggest "wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer" as recited in claims 29, 41 and 45-46. As noted above, unlike conventional devices, the claimed device has an insulator layer having a sidewall which is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer (Application at Figures 1D and 2A). Therefore, unlike conventional devices, the claimed device has an insulator layer with a sidewall angle which may be easily controlled to reduce a sharp corner stress (Application at page 8, lines 17-21).

Clearly, Okonogi does not teach or suggest these novel features. Indeed, as noted

above, Okonogi merely teaches a well-known cladding process in which an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate (Okonogi at Figures 2A-2K). Therefore, Okonogi may disclose a tapered sidewall. However, the sidewalls are not formed by forming a groove in the bulk silicon. Instead, Okonogi merely forms a silicon dioxide layer 12 on a substrate 11 and oxidizes the silicon dioxide 12 so that the "peripheral portion (side wall) of the silicon dioxide layer 12 becomes a gradual step, like a bird's beak" (Okonogi at col. 4, lines 20-22). Therefore, unlike in the claimed device which has a sidewall angle which is easily controlled when forming a groove in the bulk silicon, in the Okonogi process it would be difficult to control a sidewall angle.

Moreover, the claimed device has an insulator layer having a sidewall which is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer. Clearly, Okonogi cannot provide such a feature because Okonogi teaches that after the two substrates are "clad", the device is flipped so that elements may be formed in the second substrate. Therefore, the insulator layer in the Okonogi device will always have a narrower width on an upper surface adjacent to the elements in the SOI region.

Therefore, Applicant submits that there are elements of the claimed invention which are not taught or suggested by Okonogi. Further, Okonogi would not have been combined with Tanigawa to form the claimed invention and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 29-39 and 41-49, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed

below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 5/15/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims were amended as follows:

29. (Twice Amended) A semiconductor device comprising:

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein a sidewall of said insulator layer is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

41. (Thrice Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

an insulator layer which is formed beneath an upper portion of single crystal silicon and has at least one lateral end portion adjacent a lower portion of said single crystal silicon; and

a plurality of isolation oxides formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

wherein a sidewall of said insulator layer is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

45. (Thrice Amended) A semiconductor device comprising:

a bulk semiconductor region comprising semiconductor substrate; and

a semiconductor-on-insulator region comprising:

an insulator layer which is formed beneath an upper portion of said

semiconductor substrate and has at least one lateral end portion adjacent to a lower portion of said semiconductor substrate; and

at least one isolation oxide formed in said upper portion of said semiconductor substrate so as to form at least one island of said semiconductor substrate on an upper surface of said insulator layer,

wherein a sidewall of said insulator layer is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.

46. (Twice Amended) A semiconductor device comprising:

a single crystal silicon substrate having a lower portion and an upper portion;

an insulator layer which is formed beneath said upper portion of said single crystal silicon substrate and has at least one lateral end portion adjacent to said lower portion of said single crystal silicon substrate; and

at least one isolation oxide formed in said upper portion of said single crystal silicon substrate so as to form at least one island of said single crystal silicon substrate on an upper surface of said insulator layer,

wherein a sidewall of said insulator layer is angled so that a width said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer.